CLAIMS

What is claimed is:

1. An apparatus comprising:

   means for storing 2^{n-1} branch metric values to be used in a 1/n rate signal decoder to a storage device;

   means for loading from the storage device no more than the 2^{n-1} branch metric values to generate 2^{K-1} signal states for each of an n-bit signal value received by a communications signal decoder.

2. The apparatus of claim 1 further comprising means for performing 2^{K-2} add, compare, select (ACS) butterfly calculations corresponding to the no more than 2^{n-1} branch metric values.

3. The apparatus of claim 2 wherein the means for performing 2^{K-2} ACS butterfly calculations comprises digital signal processor (DSP) registers and accumulators being used in 16-bit computation mode.

4. The apparatus of claim 3 comprising means for evaluating two path metrics in parallel.

5. The apparatus of claim 4 wherein the means for evaluating two path metrics in parallel comprises a single vector add-subtract instruction to operate on two prior path metrics and stored branch metrics.

6. The apparatus of claim 4 wherein the means for evaluating two path metrics in parallel comprises a VITMAX instruction to compare the upper and lower 16-bit values of two 32-bit DSP registers and store the larger of the two in a third register.

7. The apparatus of claim 6 wherein the VITMAX instruction is to store two decision bits into an accumulator in order to allow a selected path metric to be tracked.

8. The apparatus of claim 7 wherein the 2^{K-2} ACS butterfly calculations are to be performed within two DSP processing cycles.

9. A method to perform a Viterbi decoding algorithm comprising:

initializing path metric buffers and trace back buffers;

evaluating branch metric (BM) kernel equations;

storing the result of the BM evaluations;

performing path metric evaluations corresponding to each BM evaluation.

10. The method of claim 9 wherein the Viterbi decoding algorithm is to be performed by a 16-state, 1/3 rate decoder.

11. The method of claim 9 further comprising performing add, compare, and select (ACS) calculations to determine a most probable next state transition for each current state of an input signal to the Viterbi decoding algorithm.

12. The method of claim 11 further comprising determining a maximum path metric values corresponding to the path metric evaluations and storing them.

13. The method of claim 12 further comprising tracing back through state transitions to determine the minimum path between each bit state decoded by the Viterbi decoding algorithm.

14. The method of claim 9 wherein the number of BM equations is no more than 4.

15. The method of claim 11 wherein the ACS calculations comprise the BM calculations and path metric calculations for each current state.

16. The method of claim 11 wherein the ACS calculations comprise path metric calculations and not BM calculations for each current state.

17. The method of claim 15 wherein the number of BM and path metric calculations are reduced by taking advantage of symmetry among a table of possible next state transitions corresponding to a received encoded signal.

18. A processor comprising:

a storage unit to store 2^{n-1} branch metric values to be used in a 1/n rate signal decoder to a storage device;

a loading unit to load from the storage device no more than the 2^{n-1} branch metric values to generate 2^{K-1} signal states for each of an n-bit signal value received by a communications signal decoder.

19. The processor claim 18 wherein the storage unit is at least one memory location and the loading unit is a memory interface unit.

20. The processor of claim 19 further comprising add, compare, and select (ACS) logic to perform 2^{K-2} ACS butterfly calculations corresponding to the no more than 2^{n-1} branch metric values.

21. The processor of claim 20 wherein the ACS logic comprises digital signal processor (DSP) registers and accumulators to be used in 16-bit computation mode.

22. The processor of claim 21 comprising path metric logic to evaluating two path metrics in parallel.

23. The processor of claim 22 wherein the path metric logic is to perform a VITMAX instruction to compare the upper and lower 16-bit values of two 32-bit DSP registers and store the larger of the two in a third register.

24. The processor of claim 23 wherein the VITMAX instruction is to store two decision bits into an accumulator in order to allow a selected path metric to be tracked.

25. The processor of claim 24 wherein the 2^{K-2} ACS butterfly calculations are to be performed within two DSP processing cycles.

26. A machine-readable medium having stored thereon a set of instructions, which if executed by a machine, cause the machine to perform a method comprising:

initializing path metric buffers and trace back buffers;

evaluating no more than 4 branch metric (BM) kernel equations;

storing the result of the BM evaluations;

evaluating path metric calculations corresponding to each BM evaluation.

27. The machine-readable medium of claim 26 further comprising instructions to determine the maximum path metric values corresponding to the path metric evaluation and store them.

28. The machine-readable medium of claim 27 further comprising instructions to trace back through state transitions to determine a minimum path between each bit state decoded by the Viterbi decoding algorithm.

29. The machine-readable medium of claim 28 further comprising instructions to reduce the number of BM and path metric calculations by taking advantage of symmetry among a table of possible next state transitions corresponding to a received encoded signal.